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Reimagining Semiconductor Development: Machine Learning Applications from Device Physics to System Architectures: Survey Paper

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ABSTRACT

The paper examines semiconductor development by evaluating the shift from conventional methods to data-based and machine-learning approaches. ITRS 2.0 presents an advanced pathway which enlarges semiconductors for contemporary marketplace needs by including application-oriented improvements and specific industry demands above Moore's Law. Performance evaluation of FinFET technology takes place at the 16-nm node by identifying key variation contributors while introducing adaptive approaches. Research analyzes the consequences of FinFET performance at the 16-nm node and demonstrates how deep learning works in computer vision and why machine learning became quick and widespread in both semiconductor production and design processes. The research examines how Graph Neural Networks improve EDA workflows through the presentation of cutting-edge machine learning methods for device performance evaluation as well as IR drop prediction and chip architecture optimization strategies across PVT ranges. This paper examines non-Von Neumann computing as well as energy-efficient accelerators for AI applications while assessing the move towards smart scalable and power-efficient semiconductor solutions.

KEYWORDS: *Microserver, Euclidean data, CNN*

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INTRODUCTION

The International Technology Roadmap for Semiconductors (ITRS) provided foundational guidance since 1990 to the semiconductor industry by specifying technology needs and directing research spending during twenty years of existence. The program aimed to boost semiconductor IC product progress through high-performance microprocessor units (MPU-HP) for servers and system-on-chip (SOC-CP) for smartphones. The technology innovations proceeded from Moore's Law which established transistor density needed to double between each generation ("node").

The traditional structure of ITRS does not properly reflect modern technological application changes because industry sectors such as data centers and mobility are driving different demands. Scientific research should incorporate systematic views into the roadmap development because this need escalates. Our paper develops an updated framework called ITRS 2.0 which goes past traditional chip-level reviews by thoroughly studying vital market requirements together with application specifications.

ITRS 2.0 supports an integrated framework which examines every element within semiconductor technology infrastructure by developing fresh system drivers, metrics that better address growing application needs across diverse domains. The updated roadmap combines smartphone and microserver generational data to understand better market requirements in reference to technological innovations. This approach presents both maintenance tools and speedup elements for semiconductor innovation which directs new developments to align with market trends and application demands.

The ITRS 2.0 marks a major advancement in semiconductor roadmap methodology that will help

organizations guide through present-day technology environments and develop future semiconductor breakthroughs[1].

The research examines in-depth process alongside statistical variability of FinFET structures at the 16-nm technology node among bulk and SOI devices. The devices feature developed structures with optimal manufacturability characteristics that fulfill performance demands of the 16-nm technology. The research examines the threshold voltage sensitivity along with OFF-current and overdrive current sensitivity of both FinFET device types due to channel length, fin-width and fin-height process variations. A strategy to enhance the SOI substrate design for decreasing SOI FinFET sensitivity to fin-width variations is presented in this work. Researchers provide a detailed evaluation of the 25-nm gate length FinFET designs based on their statistical variability characteristics such as random discrete dopants (RDDs), fin-line edge roughness, gate-line edge roughness and metal gate granularity[2].

FinFETs replaced traditional planar devices because they provide superior performance together with reduced leakage and enhanced immunity to process variations. Among FinFET designs two types stand out as shorted-gate (SG) followed by asymmetric gate-work function shorted-gate (ASG). The speed performance of standard cells built with SG technology outpaces these cells built with ASG technology at the same time the leakage power of ASG cells drops by two orders of magnitude below that of SG cells. The design formats of these two FinFET configurations remain the same although their physical dimensions remain consistent.

The methodology presented optimizes power through delay-constrained usage of ASG FinFETs due to their ultra-low leakage characteristics. Fast operation of logic circuits based on ASG technology is possible through direct application of elevated VDD supply voltage until they achieve the same timing characteristics as SG-based circuits. Consequently this dynamic power increase does not negate substantial leakage reductions that lead to total power reduction. The methodology implements a power-area balance which provides decreased total power usage from higher VDD settings despite causing a delay increase.

The design explores integrated circuits which use SG and ASG cells sharing the same VDD. Hybrid circuit designs create additional options that let designers select points throughout the performance space that connect area with delay and power usage. The benefits of our approach strengthen as temperatures increase because leakage power becomes the main power consumption factor. The total power consumption of ASG circuits operating at 1.0V reaches 47.0% below SG circuits using 0.9V while maintaining an area expansion of 6.9% at 373K.The approach delivers surprising advantages for optimizing power usage in FinFET designs primarily when delay requirements remain strict and operating temperatures are elevated[3].

Li-passivation in zigzag GaN nanoribbons significantly modifies their electronic properties, enhancing Fermi velocity and reducing effective mass to improve carrier mobility. DFT investigations further show strong gas adsorption and charge transfer, highlighting their potential as high-performance nanosensors[4-5].

Machine learning has recovered substantial interest for solving diverse complex problems by investigators who use it to anticipate wind turbine breakdowns and speed up drug development procedures. Semiconductor manufacturing together with design has shown the same pattern of increased machine learning utilization. Machine learning publications about semiconductor materials grew by almost three times from 2017 to 2018 indicating a fast expansion of adoption in this sector. Researchers have developed an extensive plan which demonstrates machine learning capabilities within semiconductor technologies. This evaluation documents present applications as well as provides strategic guidance for approaching upcoming advancements. The map outlines basic advancements together with upcoming application fields along with upcoming research pathways to boost industry and scientific personnel understanding about machine learning transformations in semiconductor systems development and production[6].

The semiconductor industry faces rising challenges because chip design complexity progresses through the influence of Moore's Law. The electronic design automation system has become essential to handle design complexity in VLSI technology by ensuring reliability and improving both scalability and delivery performance. Traditional EDA methods consume considerable resources together with extensive amounts of time yet they do not ensure optimum outcomes in every design case.

The integration of Machine Learning (ML) techniques into different phases of design flow includes placement and routing for addressing their limitations. The majority of current ML solutions use Euclidean data representations to analyze EDA components despite their natural graph structure which includes circuits and RTLs and netlists. The

lack of connection between ML methods constrains their effectiveness.

Recent research has shown that Graph Neural Networks (GNNs) establish themselves as a powerful solution to connect EDA and ML approaches. The natural graph-based data structure of EDA information gives GNNs an effective solution to directly handle design difficulties in semiconductor development. This paper examines recent research which establishes the connection between GNNs and EDA flow for chip design. The paper presents major applications of GNNs with their implementation techniques along with their demonstrated outcomes to emphasize their capability in streamlining design workflow operations[7].

Computer vision applications have fully adopted deep architectures which include convolutional structures because they deliver high-effective results. Deep learning algorithms benefit from Graphics Processing Units (GPUs) suitable for general-purpose computing because researchers now seek to utilize their computational power. Internet-based large-scale data sets now enable organizations to develop neural networks that operate with both speed and precise results.

The current research explores the existing studies dealing with computer vision techniques based on deep learning algorithms by focusing particularly on Convolutional Neural Networks (CNNs) through a systematic mapping study. A total of 119 research papers received selection for analysis. The examined studies received classification through their domain applications while being evaluated according to their network designs and learning methods and research intentions and contribution types. The research domain shows both active working activity and substantial potential which encourages future research development.

Within our investigation we select human pose estimation in video frames as a specific computer vision problem that interests us. Our research analysis led to the development of three future research possibilities. Old CNN implementations need optimization to enhance their performance levels while improving accuracy results. RNNs need to be implemented for human pose estimation purposes to enhance performance by managing temporal dynamics. The research proposes to investigate unsupervised learning methods which enable neural network training without dependent labeled data. The proposed directions seek to extend present knowledge about deep learning approaches in computer vision as part of continuous development.[8].

This research develops an innovative machine learning (ML)-guided data analysis approach which uses unprocessed metrology information to analyze FeFETs' variability behavior. Silicon-doped hafnium oxide (Si:HfO2) thin films underwent Transmission Kikuchi Diffraction (TKD) analyzes. Application of polarization maps from experiments enabled the creation of models to describe variation patterns in the ferroelectric gate stack.

A wide set of training data required simulation of multi-domain FeFETs with TCAD tools. The neural network received polarization maps as inputs and used key device metrics including high/low threshold voltage and on-state current and subthreshold slope as its output targets. The implemented model processed 3000 data samples and delivered accuracy in excess of 98%.The machine learning methodology generated results in a speed that surpassed conventional TCAD simulations by 10^6 and allowed the evaluation of 10,000 test samples. The methodology delivers quick precise data-based assessment of FeFET variability that speeds up the creation and enhancement process for upcoming ferroelectric devices.[9].

This research presents a new machine learning (ML)-based method which analyzes FeFET variability by processing unprocessed metrology data. The study implemented Transmission Kikuchi Diffraction technique for measuring polarization properties of silicon-doped hafnium oxide ($Si:HfO_2$) thin films. Polarization data generated from experiments was utilized for creating spatial models of ferroelectric polarization distribution across FeFET gate stacks.

The training dataset was built through multi-domain configurations of FeFETs in Technology Computer-Aided Design (TCAD) simulations that simulated realistic ferroelectric variations. The neural network processing system received polarization maps as inputs while generating high/low threshold voltage, on-state current and subthreshold slope values as output results. 3,000 training samples led to a high prediction accuracy of 98% or higher from the model.

This technique demonstrates great computational advantages among its main benefits. The accuracy of traditional TCAD simulations comes at the cost of a high time requirement and massive resource utilization. The trained ML model delivers predictions regarding device metrics that surpass TCAD simulation rates by more than 10^6 times per second thus making it appropriate for broad statistical investigations. The analysis of 10,000 test samples through an ML model takes only a small percentage of time compared to traditional evaluation procedures.

The applied methodology delivers swift and precise results as well as extensive scalability for assessing how material irregularities in ferroelectric substances affect device operational performance. The design and optimization process for FeFET consists of significantly faster methods because of this powerful tool which drives non-volatile memory and logic applications forward. Using machine learning for test data with metrology creates new possibilities to model semiconductor device variability in a revolutionary way[10].

The impact of excessive power supply noise (PSN) specifically IR drop creates timing violations in VLSI chips that severely affect both reliability and performance quality. Accurate PSN simulation becomes extremely time-consuming especially during the repetitive IR drop signoff verification process. We present a machine learning solution enabled for fast IR drop prediction as an answer to simulation duration problems which keeps prediction accuracy levels stable. The method builds a machine learning model for circuit design analysis during Engineering Change Order (ECO) revisions before implementation. A post-ECO circuit preserves most of its original structure so the trained model functions effectively to predict IR drop outcomes in updated designs. The method reduces the requirement to start from scratch with a whole design simulation after every design revision.

A practical approach for large-scale designs demands the use of seven lightweight feature extraction techniques which are also highly scalable. The implemented features possess the capability to capture critical circuits features needed for predicting IR drop data. The method proves its usefulness through experimental tests on an industrial design containing more than three million gates. The implemented prediction model produces results with an average error margin of 3.7 mV together with a 0.55 correlation coefficient. The proposed method provides 30 times faster execution time than typical simulation techniques run at. The framework using ML technology to predict IR drop delivers essential benefits to VLSI designers through rapid analysis of IR drop which becomes very useful during design amend iterations. Application of ML technology cuts down design turnaround times and boosts industrial production standards with solid prediction results.[11].

DFT-based studies demonstrate that Indium Nitride nanoribbons can effectively detect gases like CO, CO_2, NO, and NO_2 due to notable charge transfer and band structure modulation. Similarly, Scandium Nitride monolayers show strong adsorption sensitivity toward toxic gases such as NH_3, AsH_3, BF_3, and BCl_3. Zigzag silicon carbide nanoribbons exhibit enhanced gas sensing performance through improved electronic response to hazardous gas molecules, making them promising for advanced sensor applications[12-14].

The sub-22nm technology era demands highly complex chip designs which need hundreds to thousands of tasks and steps to reach shipment readiness. Numerous activities within this process require significant amounts of data handling along with simulation tasks that consume great amounts of time and computational power. The established engineering practice involves studying data and developing models through experience-based manual processes that operate at a slow pace and lead to inefficiencies.

The latest developments in machine learning technologies present promising automated solutions which are data-based for dealing with different technical issues. Modern chip design and validation procedures now use ML tools across their different stages which leads to faster development times and less developer work. ML models perform complex analyzes by learning from examples to eradicate verification challenges before silicon production and validate systems afterward with automated tuning enhancements. Modern chip design takes advantage of ML applications which are discussed in detail throughout this research. The identification of pre-silicon hotspots with classification models combines with inference-based bug finding to extract variation data and post-silicon timing tuning through iterative optimization and learning. Modern design problems become easier to resolve using ML methods beyond traditional approaches in every case study examined. Designers aim to reduce both the duration needed to handle vast design data quantities along with the operations involved in their understanding and response. This paper uses real-world examples to illustrate how ML changes the semiconductor sector enabling ongoing research in the fast-developing field.[15]

Advanced Machine Learning (ML) and Artificial Intelligence (AI) algorithms especially Deep Neural Networks (DNNs) and Convolutional Neural Networks (CNNs) demand efficient hardware solutions which deliver low-latency and high-throughput performance because their computational needs are growing. The traditional Von Neumann architecture faces limitations because it encounters memory restrictions in addition to ineffective data transfer operations. Non-Von Neumann computing paradigms receive heightened interest with their two major components being In-Memory Computing

(IMC) and Processing-In-Memory (PIM). The architecture enables computation inside memory units to solve standard system constraints while improving energy efficiency through data transfer reduction. The authors present an all-encompassing evaluation of advanced IMC/PIM techniques that speed up ML operations with a main focus on DNNs and CNNs. The analysis includes multiple architectural approaches with their implemented circuits and data stream designs. Different IMC/PIM solutions have achieved enhanced performance together with scalability and improved energy efficiency according to our review analysis.

We conduct an evaluation of the above architectures that compares their advantages against different performance parameters including calculation speed and memory access bandwidth utilization together with power requirements and design simpleness. новых výzkumníků v oblasti IMC postuluje službu řešení pro třídní odchýle v přiesnované akcurace spolu s mnohovrstvovala integrování a znepříjemnění compability s tradicí přímými Machine Learning frameworky.

Our analysis has enabled us to recommend practical research directions which should be explored. The practical deployment of IMC technologies benefiting from development in hybrid systems architecture and enhanced memory storage and algorithm integration work with hardware development standards. Researchers together with practitioners can use this survey to identify directions that guide both PIM/IMC development because it provides structured explanations of this field and Increasing domain-wide applications of neural networks generates strong demand for quick training processes that handle large datasets. The network intrusion detection (NID) system needs speedy training to detect attacks in extensive traffic logs. The solution for this challenge requires creating a training accelerator which depends on systolic array architecture and operates through Xilinx U50 Alveo FPGA card.

The proposed accelerator maintains equivalent accuracy to standard training methods although both forward and backward passes operate together with delayed weight update implementation. The performance of the FPGA accelerator surpasses CPU and GPU by operating at three times the CPU pace and 2.5 times the GPU pace. The FPGA achieved 11.5 times higher energy efficiency compared to the CPU as well as 21.4 times better energy efficiency than the GPU .The use of FPGA-based systolic arrays operating as training accelerators delivers major performance benefits related to speed and energy efficiency. Fast neural network training performance would increase dramatically through this method mainly for NID systems which need quick processing and reduced power usage. its capacity to transform ML hardware acceleration.[16].

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System-on-chip (SoC) design performance monitoring under process, voltage and temperature (PVT) variations stands as a major challenge because parasitic effects take precedence in advanced process nodes. Performance monitoring techniques from traditional standards depend on presumed critical paths which should be already identified before operation change events. The methods will fail when critical path detection or prediction turns out incorrect. A new machine learning-based approach for chip performance monitoring stands as this paper's main contribution since it works without requiring information about critical paths. The proposed approach delivers accurate chip performance matching throughout diverse PVT conditions giving better results than conventional monitoring approaches. The experimental data shows that our method reaches 98.5% accuracy when measuring chip performance under all PVT conditions in its worst execution scenario. The methodology delivers superior reliability and accuracy to performance monitoring systems used in modern advanced chips.[18].

Density Functional Theory (DFT) investigations reveal that Cu and Fe doping in boron nitride

nanoribbons (BNNRs) significantly enhances their electrical conductivity, making them suitable candidates for nanoscale interconnects in advanced integrated circuits. Ab-initio studies on aluminum nitride nanoribbons (AlNNRs) demonstrate their potential in implementing reconfigurable logic gates due to tunable electronic properties under external stimuli. Additionally, the design of a FinFET-based operational amplifier (Op-Amp) using 22 nm high-k dielectric technology shows promising results in reducing leakage currents and enhancing performance, offering a robust solution for low-power, high-efficiency analog circuit applications[19-21].

Reliability and speed of wirelength computations for placement depend heavily on efficient global routing approaches when the complexity of interconnections increases. The introduced routing methods use circular fixed-ordering monotonic routing and evolution-based rip-up and rerouting which deploy a high-performance two-stage cost function within a congestion-driven 2D global router. The proposed via-minimization strategy includes two effective techniques for layer assignment optimization which use congestion relaxation through layer shifting and rip-up followed by reassignment in dynamic programming-based allocators.

Our router system exhibits routing performance levels equal to those of the top two contestants from the ISPD 2008 Routing Contest and achieves comparable route quality through faster processing speeds that are 1.05× and 18.47× times faster than these routers. The layer assignment method produces vias that are fewer in number while also delivering wirelengths that are shorter compared to the conventional congestion-constrained layer assignment (COLA). Our method showcases exceptional performance effectiveness as a solution to handle advanced global routing problems[22].

Data generation at a rapid pace during the Big Data era and Internet of Things (IoT) and Internet of Everything (IoE) and Cyber Physical Systems (CPS) creates ongoing escalating needs for massive data processing and storage and transmission functions. These systems need to operate in unpredictable hazardous conditions to continuously interface with physical systems under restrictive power boundary conditions. Such systems require capabilities for high performance operation within restricted energy usage boundaries together with artificial intelligence features and robustness in self-learning capabilities.

A rapid increase in artificial intelligence (AI) investigations which include deep learning and other machine learning strategies has happened across diverse academic fields. The analysis examines both the barriers and potential chances for designing adaptive architectures that conserve energy consumption in machine learning systems. We will examine brain-inspired computational models such as approximate computing because they present substantial energy saving opportunities in these systems.

This research develops an approximation computing approach to create efficient accelerators dedicated to convolutional Deep Neural Networks (DNNs). The examination of DNN data paths at detailed levels leads to better approximate computing module selection which results in energy optimization. This work illustrates the process of developing hardware adaptive machine learning systems through a multi-objective evolutionary algorithm. We outline the main difficulties in creating machine learning hardware accelerators with low energy consumption while providing guidelines for research progress in this field.[23].

CONCLUSION

The evolution of semiconductor technologies needs multiple-layered methods that transform conventional manufacturing and fabrication methods. The industry transformation results from modern innovations that include ITRS 2.0 and FinFET variability management and ML-guided chip design. Novel machine learning technologies operate together with domain-specific issues in production and architecture to accomplish faster development schedules and better make performance predictions alongside advanced device modeling capabilities. New semiconductor systems develop with help from graph neural networks and in-memory computing and hardware accelerators to fulfill current demands for AI processing and data-intensive operations. Automated data-centric process transformations now lead design outcomes toward efficient reliable and scalable solutions because they have replaced experience-based manual modeling practices. Research moving forward needs to link computational intelligence with hardware design systems in order to sustain semiconductor innovation during the age of ubiquitous computing.

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